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PLAY BACK APPARATUS

[FIG. 1]

- 1: OPERATION SECTION
- 2: CONTROL SECTION
- 3: BUFFER MEMORY
- 4: COMPRESSION DECODER
- 5: DATA EXTRACTION CIRCUIT
- 6: RAM
- 7: DATA CORRECTION CIRCUIT
- 8: SWITCHING SW
- 9: D/A
- 10: AMP
- 11: SP
- 12: ADDRESS CONTROL SIGNAL GENERATOR
- M: SOLID STATE MEMORY
- A: COMPRESSION BIT STREAM DATA
- B: PCM AUDIO DATA (16 BITS)
- C: SPECIAL AUDIO DATA (16 BITS)
- D: BIT NUMBER CONVERSION DATA (8 BITS)
- E: TEMPORARILY STORED DATA (8 BITS)
- F: OUTPUT DATA (8 BITS)
- G: ANALOG AUDIO SIGNAL

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[FIG. 2]

21: BIT STREAM ANALYZER
22: MDCT COEFFICIENT INVERSE QUANTIZATION
23: GAIN DECODE
24; SPECTRUM ENVELOPE PLAY BACK
25: INVERSE MDCT
26: MDCT COEFFICIENT INVERSE NORMALIZATION
A: COMPRESSION BIT STREAM DATA INPUT
B: MDCT COEFFICIENT QUANTIZATION INDEX
C: GAIN QUANTIZATION INDEX
D: SPECTRUM ENVELOPE QUANTIZATION PARAMETER
E: WINDOW INFORMATION
F: PCM AUDIO DATA OUTPUT

[FIG. 3]

A: RAM ADDRESS SPACE

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[FIG. 4]

- 2: CONTROL SECTION
- 4: COMPRESSION DECODER
- 5: DATA EXTRACTION CIRCUIT
- 6: RAM
- 7: DATA CORRECTION CIRCUIT
- 8: SWITCHING SW
- 12: ADDRESS CONTROL SIGNAL GENERATOR
- A: FROM BUFFER MEMORY 3
- B: PCM AUDIO DATA (16 BITS)
- C: BIT NUMBER CONVERSION DATA (8 BITS)
- D: TEMPORARILY STORED DATA (8 BITS)
- E: SPECIAL AUDIO DATA (16 BITS)
- F: OUTPUT DATA (8 BITS)
- G: TO D/A CONVERTER 9

[FIG. 5]

- A: PCM CLOCK
- B: BIT NUMBER CONVERSION DATA
- C: WE SIGNAL
- D: ADR SIGNAL (AT THE TIME OF DATA WRITING)

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[FIG. 6]

A: PCM CLOCK
B: ADR SIGNAL (AT THE TIME OF DATA READING)
C: RE SIGNAL
D: OUTPUT DATA

[FIG. 7]

A: PCM CLOCK
B: ADR SIGNAL (AT THE TIME OF DATA READING)
C: RE SIGNAL
D: OUTPUT DATA

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[FIG. 8]

- S1: TEMPORARILY STORED DATA EXISTS IN RAM 6 ?
- S2: READ OUT DATA OF FIXED MEMORY AND STORE AND HOLD TEMPORARILY
STORED DATA IN RAM 6
- S3: PLAY BACK COMMAND IS GIVEN ?
- S4: SELECT DATA READING OUT START POSITION
- S5: START DATA PLAY BACK FROM READING OUT START POSITION
- S6: PLAY BACK STOP COMMAND IS GIVEN ?
- S7: FF COMMAND IS GIVEN ?
- S8: REW COMMAND IS GIVEN ?
- S9: DATA IS COMPLETED ?
- A: FROM FF PROCESSING ROUTINE
- B: FROM REW PROCESSING ROUTINE
- C: TO FF PROCESSING ROUTINE
- D: TO REW PROCESSING ROUTINE

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[FIG. 9]

A: FF PROCESSING START

B: FF PROCESSING END RETURN

S11: OUTPUT STOP FROM COMPRESSION DECODER 4

S12: READING OUT OPERATION OF TEMPORARILY STORED DATA OF RAM
6

S13: SWITCH SWITCHING SW 8 TO OUTPUT SIDE OF DATA CORRECTION
CIRCUIT 7

S14: FF COMMAND IS RELEASED ?

S15: CALCULATE DATA READING OUT START POSITION X1

S16: RESTART OF OUTPUT FROM COMPRESSION DECODER 4

S17: WRITING OPERATION OF TEMPORARILY STORED DATA OF RAM 6

S18: SWITCH SWITCHING SW 8 TO OUTPUT SIDE OF COMPRESSION DECODER
4

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[FIG. 10]

A: REW PROCESSING START

B: REW PROCESSING END RETURN

S21: OUTPUT STOP FROM COMPRESSION DECODER 4

S22: READING OUT OPERATION OF TEMPORARILY STORED DATA OF RAM
6

S23: SWITCH SWITCHING SW 8 TO OUTPUT SIDE OF DATA CORRECTION
CIRCUIT 7

S24: REW COMMAND IS RELEASED ?

S25: CALCULATE DATA READING OUT START POSITION X2

S26: RELEASE STORE AND HOLDING TEMPORARILY STORED DATA OF RAM
6

S27: RESTART OF OUTPUT FROM COMPRESSION DECODER 4

S28: SWITCH SWITCHING SW 8 TO OUTPUT SIDE OF COMPRESSION DECODER
4

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[FIG. 11]

- 1: OPERATION SECTION
- 3: BUFFER MEMORY
- 4: COMPRESSION DECODER
- 5: DATA EXTRACTION CIRCUIT
- 6: RAM
- 7: DATA CORRECTION CIRCUIT
- 8: SWITCHING SW
- 9: D/A
- 10: AMP
- 11: SP
- 12: ADDRESS CONTROL SIGNAL GENERATOR
- 14: CONTROL SECTION
- M: SOLID STATE MEMORY
- A: COMPRESSION BIT STREAM DATA
- B: PCM AUDIO DATA (16 BITS)
- C: SPECIAL AUDIO DATA (16 BITS)
- D: BIT NUMBER CONVERSION DATA (8 BITS)
- E: TEMPORARILY STORED DATA (8 BITS)
- F: OUTPUT DATA (8 BITS)
- G: ANALOG AUDIO SIGNAL
- H: DEFAULT DATA (8 BITS)

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[FIG. 12]

S1: TEMPORARILY STORED DATA EXISTS IN RAM 6 ?

S32: READ OUT DEFAULT DATA OF ROM 13 AND STORE AND HOLD
TEMPORARILY STORED DATA

S3: PLAY BACK COMMAND IS GIVEN ?

S4: SELECT DATA READING OUT START POSITION

S5: START DATA PLAY BACK FROM READING OUT START POSITION

S6: PLAY BACK STOP COMMAND IS GIVEN ?

S7: FF COMMAND IS GIVEN ?

S8: REW COMMAND IS GIVEN ?

S9: DATA IS COMPLETED ?

A: FROM FF PROCESSING ROUTINE

B: FROM REW PROCESSING ROUTINE

C: TO FF PROCESSING ROUTINE

D: TO REW PROCESSING ROUTINE

【書類名】 図面

Q64051

【図1】

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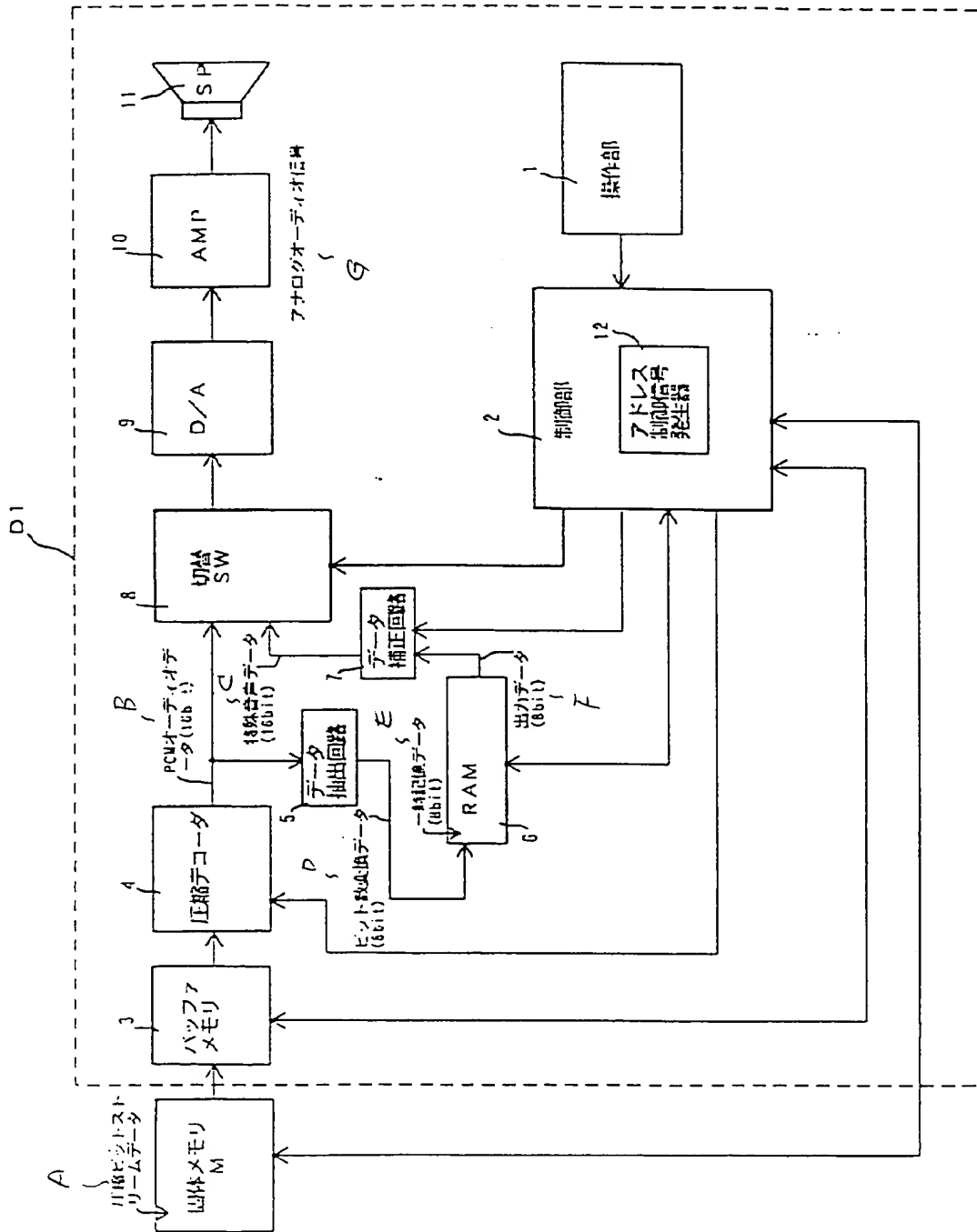


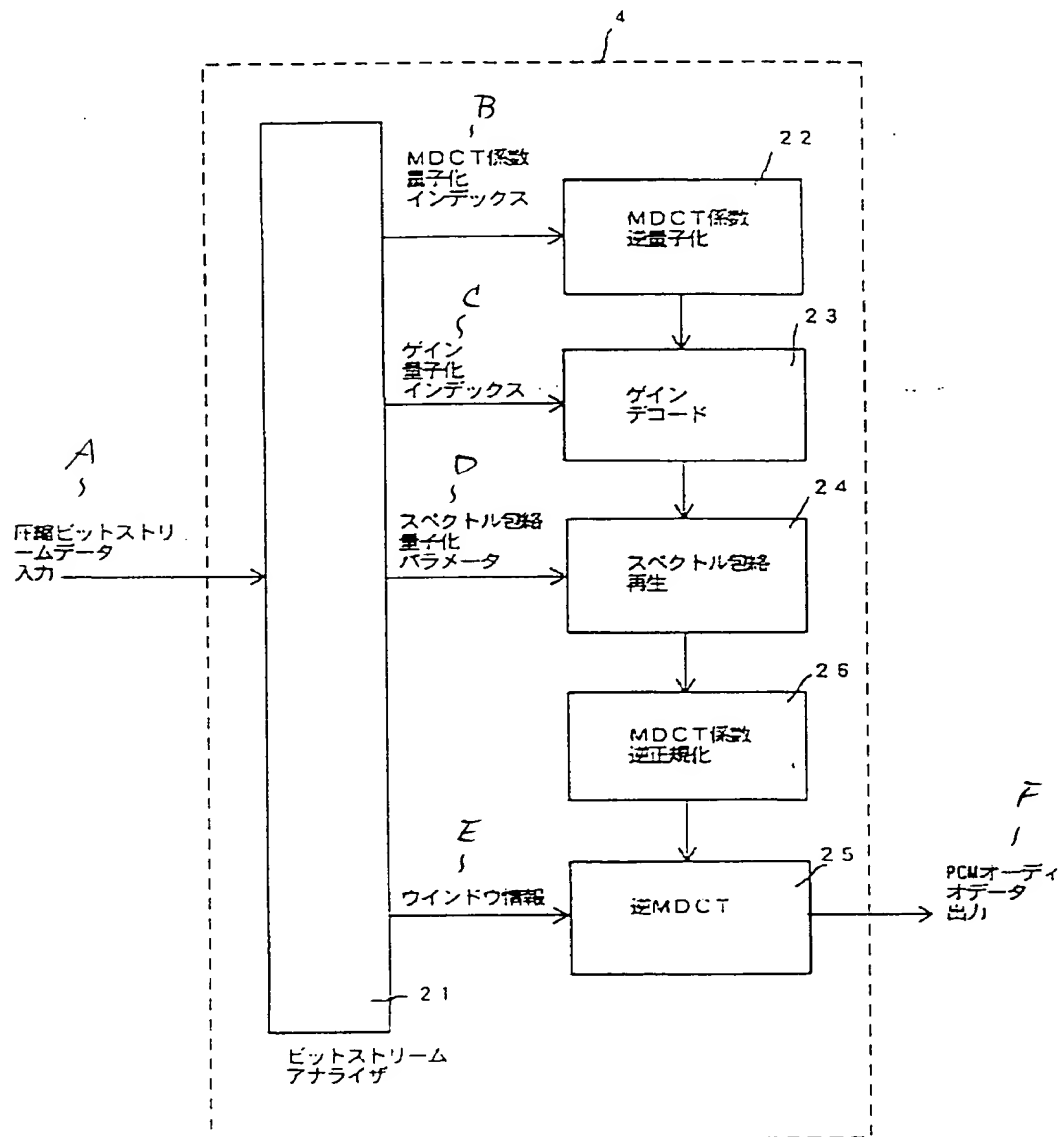
Fig. 1

【図2】

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Fig. 2

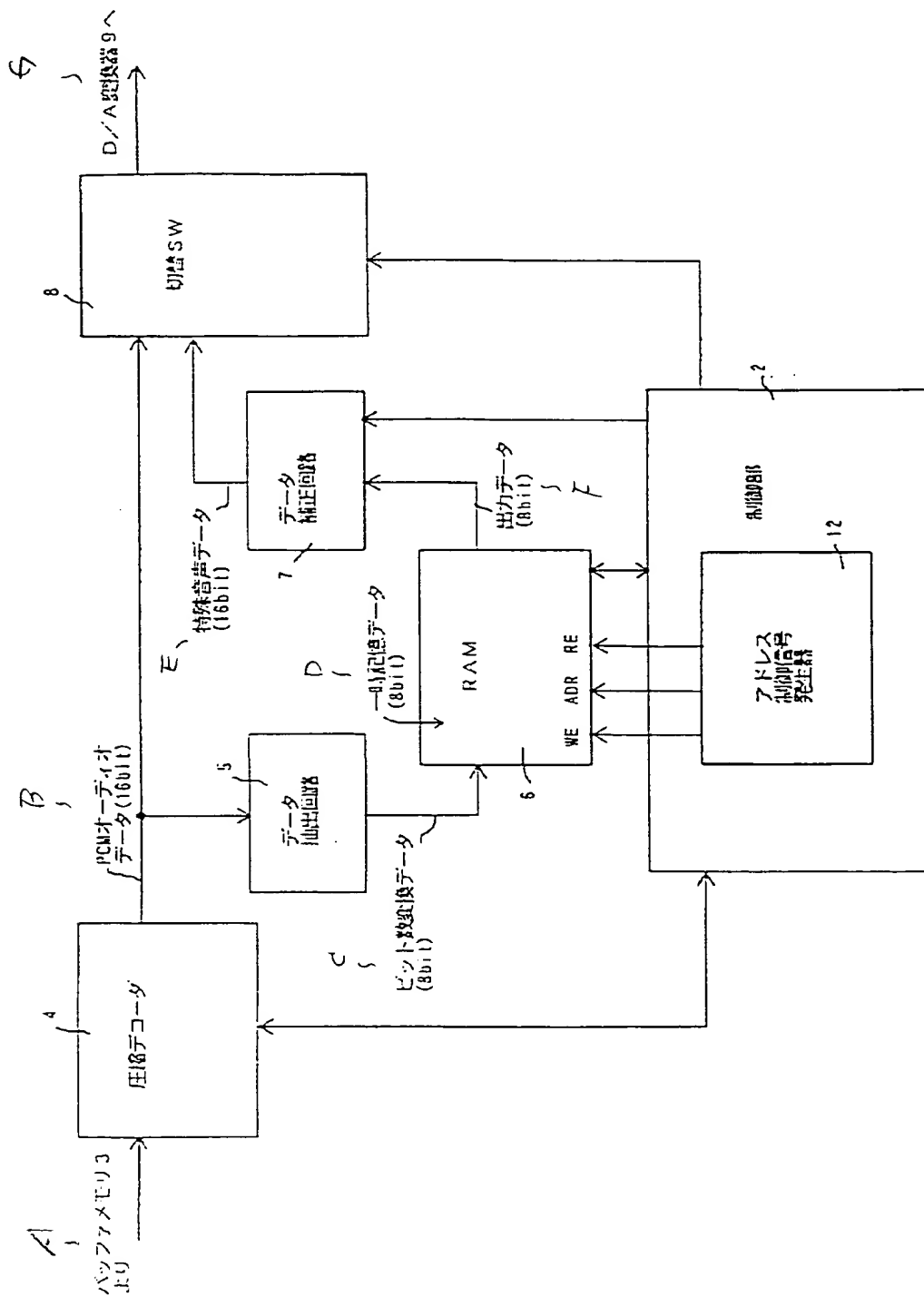


〔図4〕

Q64051

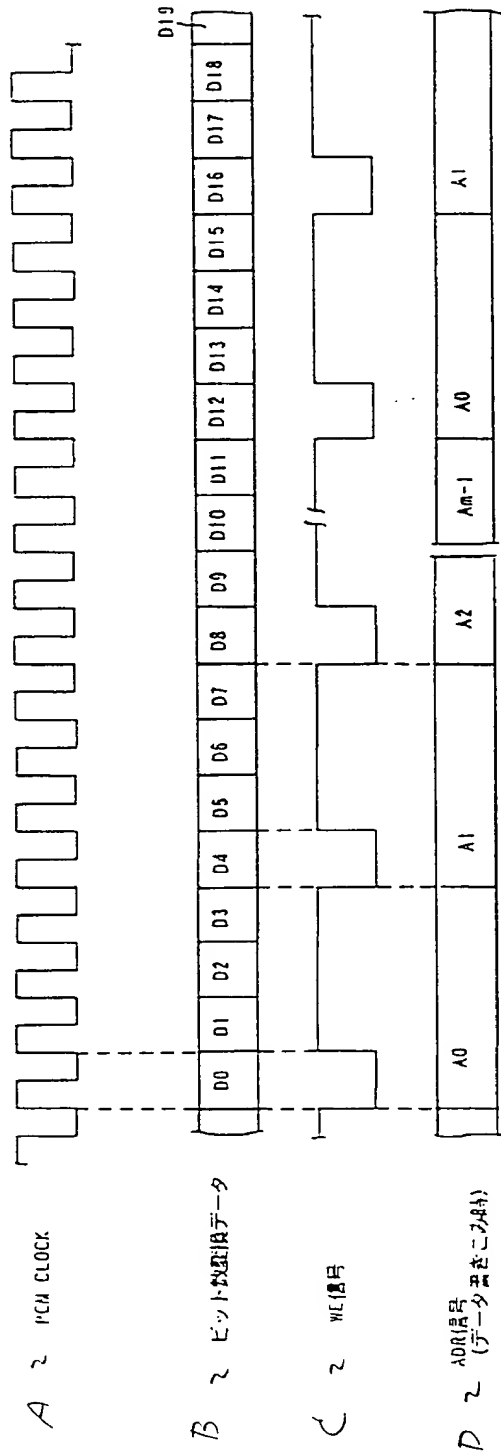
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Fig. 4



【図5】

Fig 5



—【図 6】—

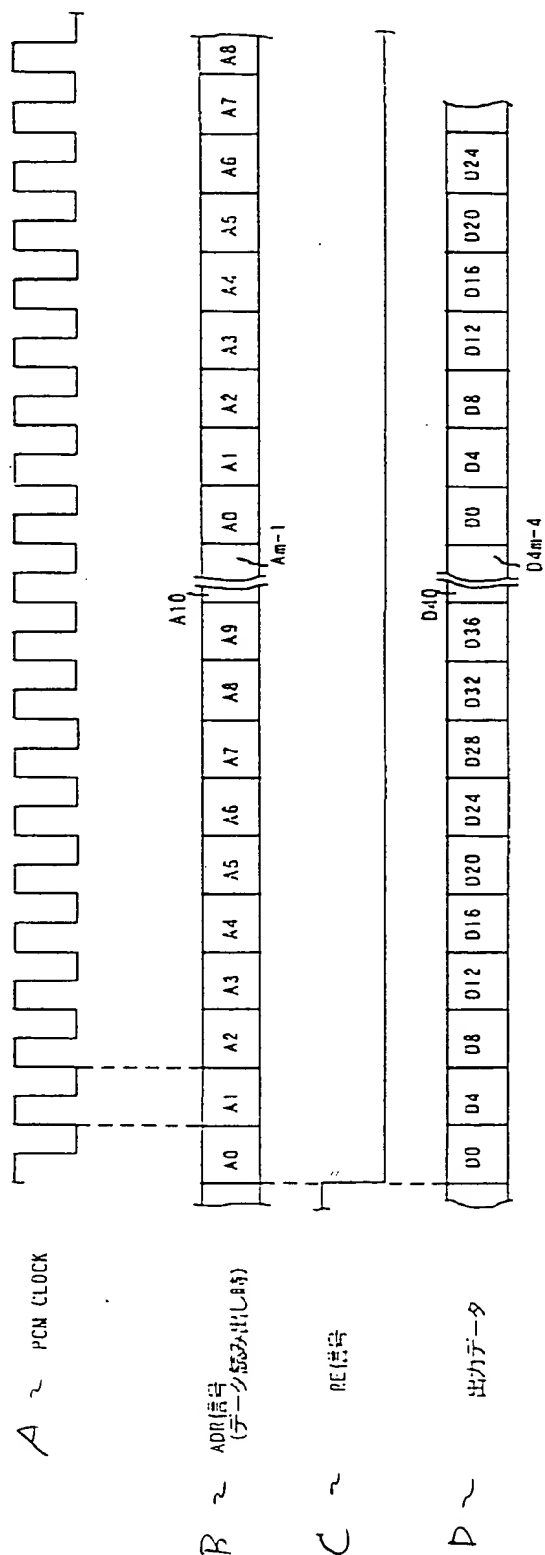


Fig 6

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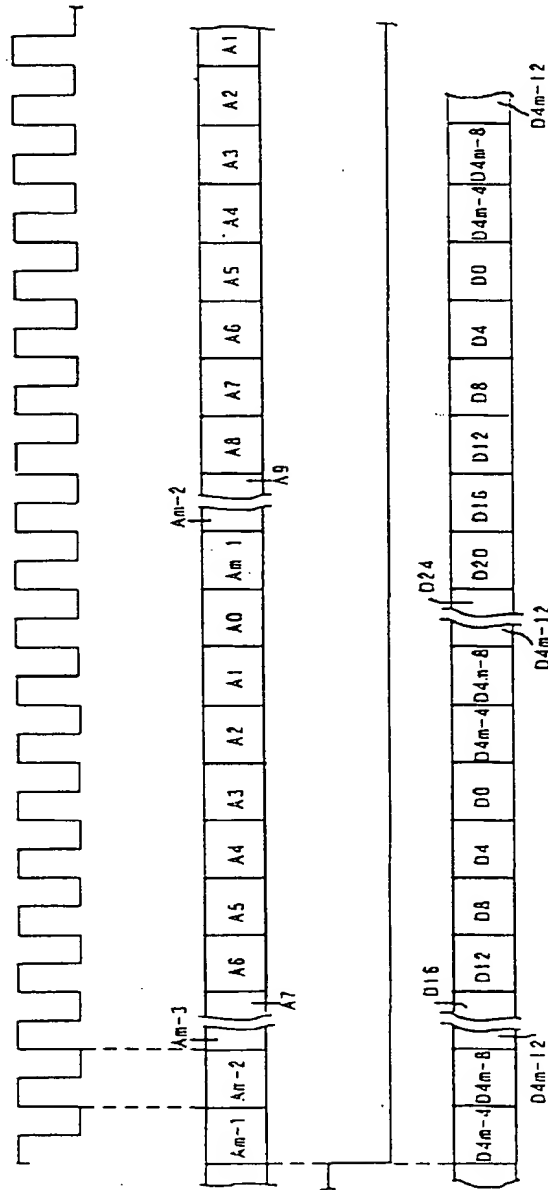
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[図7]



A ~ PCM CLOCK

B ~ AUX (データ読み出し)

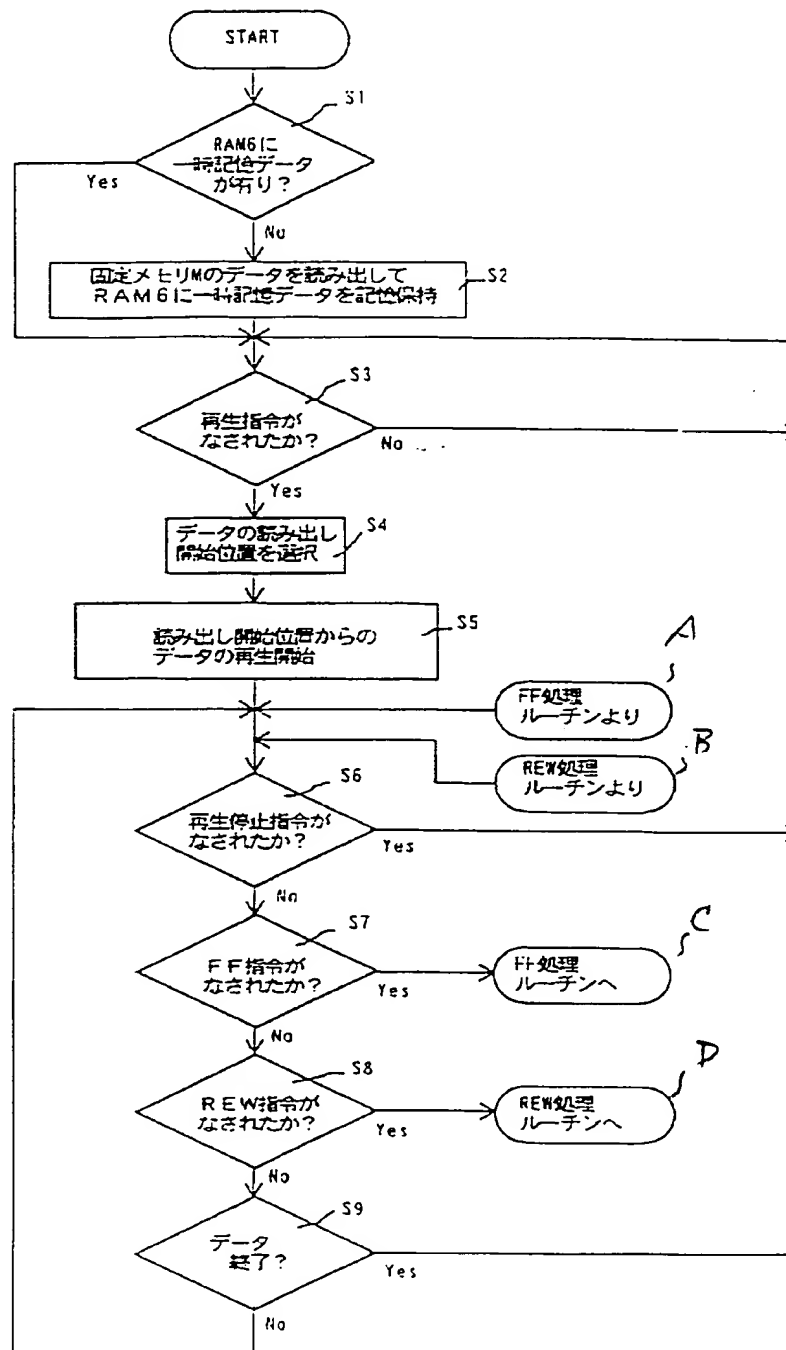
C ~ RE信号

D ~ 出力データ

Fig. 7

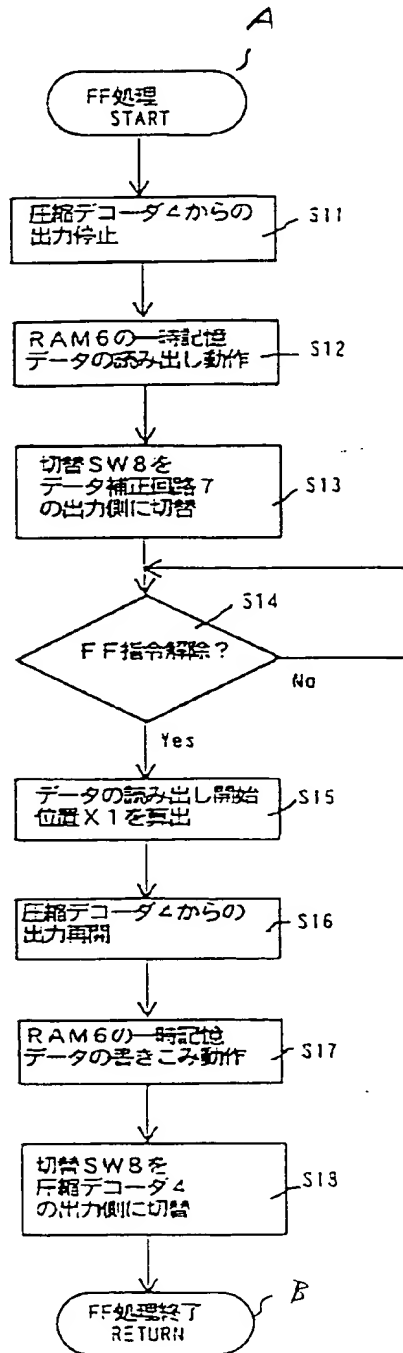
〔図8〕

Fig. 8



【図9】

Fig. 9



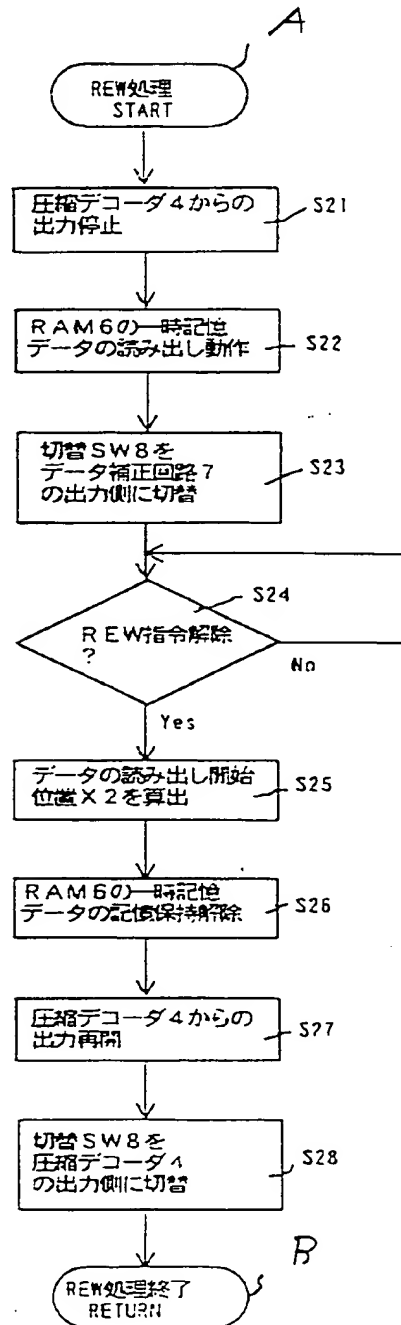
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【図10】

Fig. 10





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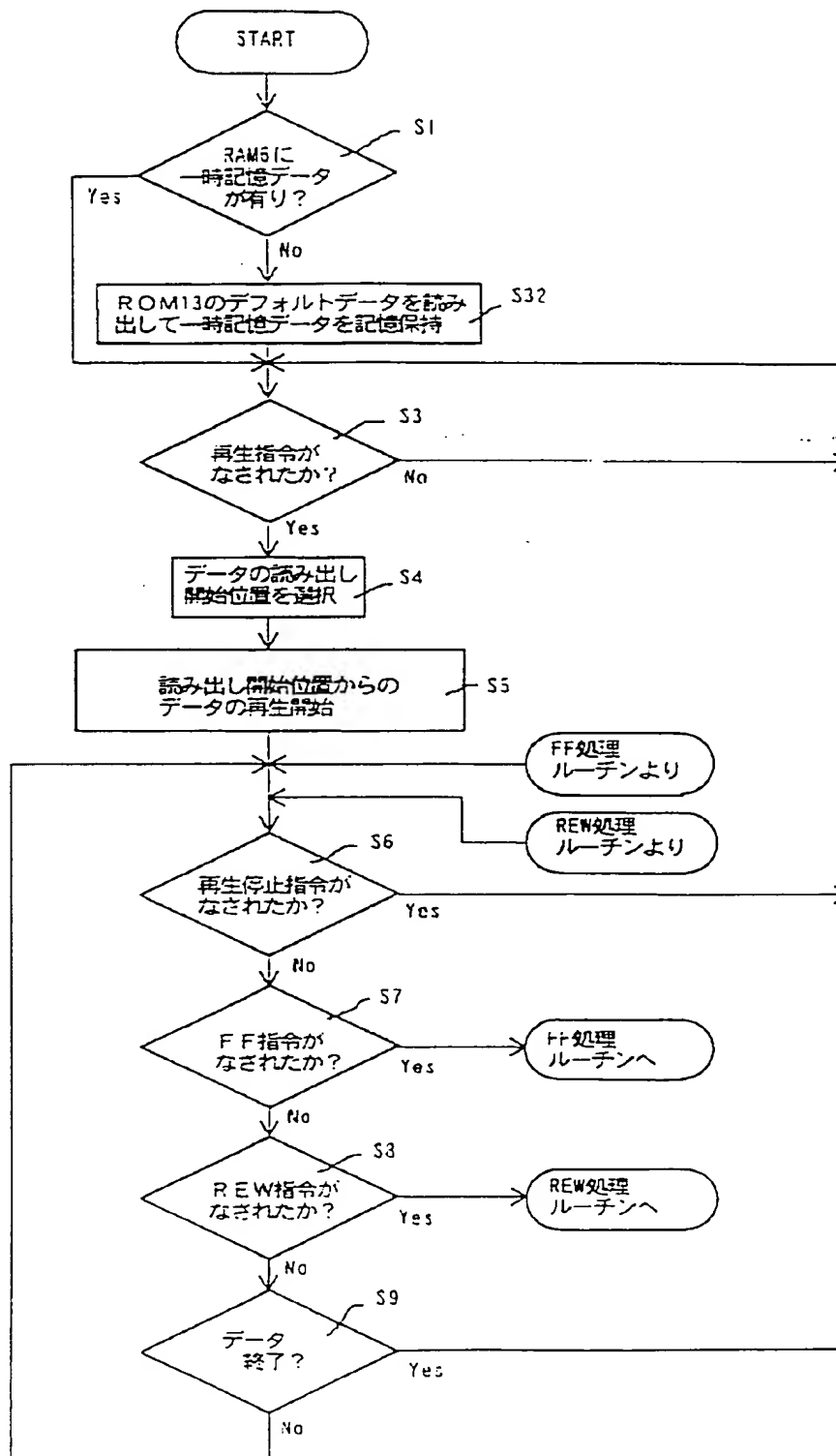
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Fig. 12



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{図13}

Fig. 13

